ABSTRACT

This invention provides practical methods to make a DRAM fully compatible with existing SRAM products~~. This is~~ accomplished by design and manufacture methods ~~according to the invention,~~ which includes a method to reduce standby power of reference voltage generators and a method to avoid the alpha particle problem using a novel error correction code (ECC) mechanism. The reference voltage generator of the present invention can adjust the values of output voltage and driving power separately following simple procedures. It has very strong driving power to maintain the reference voltage, which is necessary to support high-speed operation of memory devices of the present invention. In the mean time, its standby power can be reduced by orders of magnitudes using simple control mechanism, which is necessary to make our memory device compatible with the properties of existing SRAM products. There is no need to use feedback circuits or operation amplifiers, so the circuit is extremely stable and reliable. ~~It is an ideal reference voltage generator to generate the bit line pre-charge voltage for a DRAM designed to emulate an SRAM device. The unique features of the ECC protection of the present invention avoid RC delay problems in prior art ECC circuits, which is necessary to support high speed operation of our products. The alpha particle problem is no longer an issue. All the supporting circuits can use repeated layouts, which is very important for memory design. The manufacture technology for embedded IC is simplified dramatically, which allow us to have high performance logic circuits. The memory devices of the present invention are therefore compatible in every detailed feature with existing SRAM products.~~

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November 28, 2003